AMENDMENT TO THE CLAIMS

This listing of claims will replace all prior versions of claims in the application.

Listing of Claims:

1. (currently amended) In an integrated circuit multiprocessor switching device, an apparatus for mapping a plurality of ~~interrupt sources~~ interrupts and a plurality of virtual channels ~~to a particular one of a~~ through a packet manager to route data packets between external devices and a plurality of processors, comprising:

an interrupt status register for storing the interrupts;

mask registers associated with the virtual channels for selectively masking contents of the interrupt status register for each of the virtual channels, the virtual channels for routing the data packets;

a merged interrupt indication register associated with each virtual channel for storing ~~merged and~~ masked interrupt values for the virtual channels that are obtained after masking and merging the contents of the interrupt status register with the mask registers;

an interrupt mapping register associated with each virtual channel for storing a processor identification for routing masked interrupt value of a respective virtual channel to a selected processor of the plurality of processors;

a demultiplexing circuit coupled to the merged interrupt indication register and the interrupt mapping register for coupling the ~~merged and~~ masked interrupt value for each virtual channel to ~~the selected processor~~ a corresponding one of the selected processors to selectively route the masked interrupt values in the packet manager.

2. (currently amended) The apparatus recited in claim 1 formed in ~~a packet manager~~ an input circuit of the packet manager for mapping a plurality of interrupts associated with input of a data packet.

3. (currently amended) The apparatus recited in claim 1 formed in ~~a packet manager~~ an output circuit of the packet manager for mapping a plurality of interrupts associated with output of a data packet.

4. (previously presented) The apparatus recited in claim 1 formed in a system controller for processing interrupts associated with data packets.

5. (canceled)

6. (previously presented) The apparatus recited in claim 1 wherein the mask registers are programmable to select which interrupts are masked.

7. (previously presented) The apparatus recited in claim 1, wherein the selected processor identified by the processor identification determines an interrupting channel by running an interrupt service routine that first reads the merged interrupt indication register to identify a virtual channel associated with an interrupt and then reads the interrupt status register to determine a respective interrupt.

8. (previously presented) The apparatus recited in claim 1, wherein the interrupt mapping register further includes a priority level indication associated with each virtual channel for prioritizing any interrupt issued.

9. (currently amended) An interrupt mapper in a packet manager for mapping interrupts for a plurality of virtual channels to a plurality of processing cores to route data packets between the processing cores and external devices, comprising:

a plurality of interrupt registers, where each interrupt register identifies an interrupt for one or more of the plurality of virtual channels, the virtual channels for routing the data packets;

a mask register associated with each of the plurality of interrupt registers for selectively masking contents of the interrupt register to generate a masked interrupt for each virtual channel;

a channel merge circuit for merging the masked interrupt for each virtual channel into an interrupt indication value for each respective virtual channel;

a channel register that stores the interrupt indication values for the plurality of the virtual channels;

a plurality of processor map storage devices, each processor map storage device storing a processor identification value for respective one of the plurality of virtual channels; and

a demultiplexer coupled to the channel register and the plurality of processor map storage devices for mapping each interrupt indication value for a virtual channel to a corresponding one of the selected ~~one of the~~ processing cores identified by the processor identification for that respective virtual channel to selectively route the interrupt indication values in the packet manager.

10. (previously presented) The interrupt mapper as recited in claim 9, wherein the channel merge circuit includes a plurality of AND gates coupled to the interrupt registers and the mask register for generating the masked interrupt for each virtual channel.

11. (previously presented) The interrupt mapper as recited in claim 9, wherein each processor map storage device stores a processor identification value and a priority level for respective one of the plurality of virtual channels.

12. (previously presented) The interrupt mapper as recited in claim 9, wherein the channel merge circuit comprises OR gate circuitry for merging the masked interrupts into an interrupt indication value for each virtual channel.

13. (previously presented) The interrupt mapper as recited in claim 9, wherein a processing core that receives an interrupt reads the channel register to determine which virtual channel is associated with an interrupt and then reads the plurality of interrupt registers to determine a respective interrupt source.

14. (previously presented) The interrupt mapper as recited in claim 13, wherein the plurality of interrupt registers and the channel register are each sized to match a processing width of the processing core.

15. (previously presented) The interrupt mapper as recited in claim 14, wherein the selected processing core determines the source of an interrupt with two register reads.

16. (previously presented) The interrupt mapper as recited in claim 9, wherein an interrupt associated with each virtual channel is mapped to only one processing core.

17. (previously presented) The interrupt mapper as recited in claim 9, wherein the plurality of processor map storage devices are programmable to dynamically assign a processing core to a given virtual channel to implement load balancing among the processing cores.

18-20. (canceled)